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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,209	LINGUNIS ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-17* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I claims 1 – 16 in the reply filed on October 31, 2004 is acknowledged.

Response to Arguments

2. Applicant's arguments with respect to claims 1 – 8 and 10 – 16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1 – 3, 7, 10, 14, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd, US 6,461,529 in view of Huang, "Very Low Defects and High Performance Ge – On – Insulator p – MOSFETs with Al_2O_3 Gate Dielectrics", 2003 Symposium on VLSI Technology Digest of technical papers, p 119 – 120 (10 – 12 June, 2003).

Regarding claims 1, 3, 10 and 16, Boyd teaches a method of forming a semiconductor device, the method comprising the steps of:

- forming a dielectric layer 135 over a substrate 130 (Fig. 5G),
- forming a mask layer 131 + 138 of silicon nitride over the dielectric layer 135 (Fig. 5G),
- patterning the mask layer (Fig. 5G) to form a mask including a mask line 131 and space pattern 140, the mask line and space pattern including at least one mask space (Fig. 5G), and
- forming a conductive layer 141 in the at least one mask space (Fig. 5I), the conductive layer 141 includes a width dimension about equal to the width dimension of the least one mask space (Fig. 5J) in between column 7, line 23 and column 9, line 42.

Boyd fails to teach wherein the substrate comprises a germanium-on-insulator

(GOI) structure including a semiconductor substrate; an insulating layer disposed over the semiconductor substrate and a semiconductor layer comprising crystalline germanium (Ge) disposed over the insulating layer.

Huang teaches that pure crystalline Ge channel MOSFETs fabricated on GOI substrate have the benefit of increased hole mobility over the Si channel MOSFETs in column 1, page 119 under the heading "**Introduction**".

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boyd and form the semiconductor device on a GOI substrate have the benefit of enhanced hole mobility over the Si channel MOSFETs as taught by Huang in column 1, page 119 under the heading "Introduction".

Regarding claim 2, Boyd teaches the steps of removing the mask to expose sidewalls of the conductive layer, wherein the sidewalls include relatively smooth surfaces with respect to Fig. 5K in column 9, lines 57 – 61.

Regarding claim 7, Boyd teaches that a CMOS device can be formed using standard CMOS technology with source and drain in between column 9, line 56 and column 10, line 8 which will inherently have the a gate stack formed on the substrate including an active layer interposed between a source and a drain, the gate stack including: the gate dielectric layer disposed over the substrate, and the conductive layer disposed over the gate dielectric layer.

Regarding claim 14, Boyd teaches the mask defines a pitch of the mask line and space pattern with reference to Fig. 5G.

Regarding claim 15, Boyd teaches forming a conformal layer of a conductive material 141 over the mask 138 and exposed surface of the dielectric layer 149; and anisotropically etching to remove a portion of the conductive material from horizontal surfaces of the mask with reference to Figs 5I and 5J.

7. Claims 1 – 3, 6, 10, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sitaram, US 6,723,657 in view of Huang, "Very Low Defects and High Performance Ge – On – Insulator p – MOSFETs with Al_2O_3 Gate Dielectrics", 2003 Symposium on VLSI Technology Digest of technical papers, p 119 – 120 (10 – 12 June, 2003).

Regarding claims 1, 3, 6, 10, 13 and 16, Sitaram teaches a method of forming a semiconductor device, the method comprising the steps of:

- forming a gate dielectric layer 11 of silicon oxide over a substrate 10 (Fig. 2),
- forming a mask layer 13 of silicon nitride over the dielectric layer 11 (Fig. 2),
- patterning the mask layer (Fig. 2) to form a mask including a mask line and space pattern, the mask line (the formation of the mask line is inherent in the process since the mask pattern is formed over the entire wafer to form multiple gates of multiple chips) and space pattern including at least one mask space (Fig. 2), and
- forming a conductive layer 16 in the at least one mask space (Fig. 2), the conductive layer 16 includes a width dimension about equal to the width dimension of the least one mask space in column 2, lines 49 – 67.

Sitaram fails to teach wherein the substrate comprises a germanium-on-insulator

(GOI) structure including a semiconductor substrate; an insulating layer disposed over the semiconductor substrate and a semiconductor layer comprising crystalline germanium (Ge) disposed over the insulating layer.

Huang teaches that pure crystalline Ge channel MOSFETs fabricated on GOI substrate have the benefit of increased hole mobility over the Si channel MOSFETs in column 1, page 119 under the heading "**Introduction**".

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sitaram and form the semiconductor device on a GOI substrate have the benefit of enhanced hole mobility over the Si channel MOSFETs as taught by Huang in column 1, page 119 under the heading "Introduction".

Regarding claim 2, Sitaram teaches the steps of removing the mask to expose sidewalls of the conductive layer, wherein the sidewalls include relatively smooth surfaces with respect to Fig. 5 in column 3, lines 22 – 27.

Regarding claim 14, Sitaram teaches the mask defines a pitch of the mask line and space pattern with reference to Fig. 2.

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd, US 6,461,529 or Sitaram, US 6,723,657 in view of Huang, "Very Low Defects and High Performance Ge – On – Insulator p – MOSFETs with Al_2O_3 Gate Dielectrics", 2003 Symposium on VLSI Technology Digest of technical papers, p 119 – 120 (10 – 12 June, 2003) as applied to claim 1 above, and further in view of "Shipley Announces New Dual Purpose Spin – On Anti-Reflection Coating for Device Fabrication." New Release from www.rohmhass.com, May 2002.

Boyd or Sitaram fails to teach forming and patterning an ARC layer over the mask layer.

Shiply's news release teaches the benefit of using ARC coating during trench etching (see paragraph 3 of the news release) by eliminating the formation of fences.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boyd or Sitaram and form an ARC layer on the mask layer for the benefit of eliminating the formation of fences during trench (mask space) formation as taught by Shiply in paragraph 3 of the news release.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd, US 6,461,529 in view of Huang, "Very Low Defects and High Performance Ge – On – Insulator p – MOSFETs with Al_2O_3 Gate Dielectrics", 2003 Symposium on VLSI Technology Digest of technical papers, p 119 – 120 (10 – 12 June, 2003) as applied to claim 7 above, and further in view of Clevenger; US 6,563,160.

Boyd fails to teach a gate dielectric having permittivity greater than silicon dioxide.

Clevenger teaches that devices with high – k dielectric are beneficial for reducing equivalent gate oxide thickness therefore improving reliability in column 1, lines 61 - 67.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boyd and replace the gate oxide with gate dielectric having permittivity greater than silicon dioxide for the benefit of reducing equivalent gate oxide thickness therefore improving reliability as taught by Clevenger in column 1, lines 61 - 67.

10. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd, US 6,461,529 in view of Huang, "Very Low Defects and High Performance Ge – On – Insulator p – MOSFETs with Al_2O_3 Gate Dielectrics", 2003 Symposium on VLSI Technology Digest of technical papers, p 119 – 120 (10 – 12 June, 2003) as applied to claim 1 above, and further in view of Hsieh, US 2003/0109111.

Boyd teaches a method for forming the conductive layer of a gate by etching a mask layer over a dielectric using a damascene etch scheme for the benefit of etching high aspect ratio while retaining high selectivity in column 2, lines 35 – 42, but fails to teach the dielectric layer comprises a charge-trapping dielectric layer, wherein the charge-trapping dielectric layer includes a tunneling layer; a charge-trapping layer, and an insulating layer, wherein the tunneling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunneling layer and the insulating layer is disposed over the charge-trapping layer.

Hsieh teaches a flash memory structure with reference to Fig. 4 where conductive layer 108 id formed over dielectric layer comprising a charge-trapping dielectric layer, wherein the charge-trapping dielectric layer includes a tunneling layer; a charge-trapping layer, and an insulating layer, wherein the tunneling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunneling layer and the insulating layer is disposed over the charge-trapping layer.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boyd and form the gate conductive layers of Hsieh's device by forming the conductive layer of a gate by etching a mask layer over a

dielectric using a damascene etch scheme for the benefit of etching high aspect ratio while retaining high selectivity as taught by Boyd in column 2, lines 35 – 42.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

This application contains claim 17 drawn to an invention nonelected with traverse in Paper filed on October 31, 2004. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571 272 1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
November 29, 2004

Patent Examiner